8/12/93

Bizzat Comments?

IR & D HISTORY: PARALLEL PROCESSOR COMMUNICATION

1989 IR&D -

None.

Planned 1990 objective: "Enhance the hypercube routing algorithm to accommodate non-power-of-2 cube configurations"

Planned 1990 approach: "Enhance the routing and broadcast algorithms for the hypercube to improve its ability to tolerate faulty nodes and allow for degraded operation.

1990 IR&D -

Title: Hypercube Interconnectivity Improvement

Tasks:
1) Literature search to identify algorithms
2) Develop HOL model
3) Develop ADAS model
4) Develop register transfer model
5) Develop router spec
6) Final report

PI: Norm Tinklepaugh

Funding: $89K plus $100K reserve Expended @ 12/31/90 $83K, with reserve not allocated, work halted in Nov.

Synopsis: Task 1 identifies the "standard" hypercube routing algorithm (e-cube). An MSD algorithm is also derived that appends an "extra dimension" on the nose and the tail of the route to supply adaptive routing if busy (failed). HOL model produced, ADAS model spec'd and produced via RTI. An algorithm was developed to down-size the hypbercube to smaller structures (incomplete hypercubes) that still have complete connectivity with the MSD algorithm.

ADAS model eventually excercised on SQQ-89 TA beamformer algorithms (see 1991), but no tuning or validation performed. No definitive output.

This IR&D also funds design enhancement of iPSC serial channels to produce up to 40 Mbps, an improvement over the orig. 22.8 Mbps

Items 4,5, & 6 were not produced.

Comment: Effort concentrated on routing algorithm development for the hypercube. Results for incomplete hypercubes significant, but not applicable to the evolving topology. Unfortunately, the possibilities of deadlock limit the usefulness of the adpative algorithm studied. Mechanization via a link design and communication protocol is yet to be done.

SRC Subtask

Title: Hypercube Router

Tasks: "Evalute the algorithm developed by MSD for routing messages in a hypercube with failed nodes, where the cube may be a non-power-of-two size."

PI: Rakesh Jha (SRC)

Funding: $10K (from MSD IR&D funding above)

Synopsis: Verify MSD algorithm connectivity. Look into the deadlock potential of algorithm. Plans for: 1) proof of deadlock potential, 2) recommendations for non-power-of-two expansion, 3) develop algorithm to deal with busy (as opposed to failed) nodes

Comment: Examples of deadlock using the MSD algorithm presented, no completed proof. Out of funds before success on items 2) or 3) completed. This leaves the adequacy and applicability of the MSD algorithm development uncertain.

1991 IR&D -

Title: Accelerated Hypercube ADAS Model

Tasks: "Provide technical guidance on the adaptation of the ADAS modeling tool in support of the SQQ-89(I) performance modeling of the accelerated hypercube architecture."

PI: Tony Niolu

Funding: $30K spent $24K @ 7/15/91

Synopsis: Contract with RTI to continue to adapt the ADAS model to represent the proposed SQQ-89(I) architecture. At 7/15/91: spec complete and model development underway. Algorithm development not started. Final report contains sample output from working simulation, but model not tuned. No use of model to evaluate design or influence further development.

Comment: This work only peripherally connected to the parallel processor communications issue. ADAS modeling has not been applied to any other application or processor in support of communications development - hence at this time is a dead end from the point of view of parallel processor communications.

1992 IR&D -

None?

1993 IR&D -

Title: Parallel Processor Software Tools and Applications

Tasks:
1) Develop workstation based multi-cell debugger
2) Obtain and evaluate SPOX 1.4
3) Develop interprocessor communication management techniques based on an existing COTS real-time operating system.
4) Develop Sun-based board support packages

Task (3) technical approach: "Obtain and evaluate Spectron's current C40-based real

time operating system (SPOX 1.4) which provides communication drivers. Work directly with Spectron to evaluate and test various communication techniques (eg. wormhole routing), choose the best methods and provide these libraries to them for integration into their product line."

PI: Brent Smith

Funding: Task (2&3): $60K (20K design, 40K implementation) Expended at 8/x/93: $yyK

Synopsis: Task (3) addresses parallel processor communication. Steps backward are taken to re-define operating system choice. Routing algorithm choices re-studied. Reccommended we define limited deterministic routing using Spectron application note. Preliminary design provided to use "TI router" under SPOX to provide general deterministic routing for MX16.

Comment: No work with Spectron to modify their operating system for parallel processor communication. Solution to the general adaptive/fault tolerant routing question postponed. However proposals provide solutions not only to the routing question but also to the protocol and device driver layer issues.

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